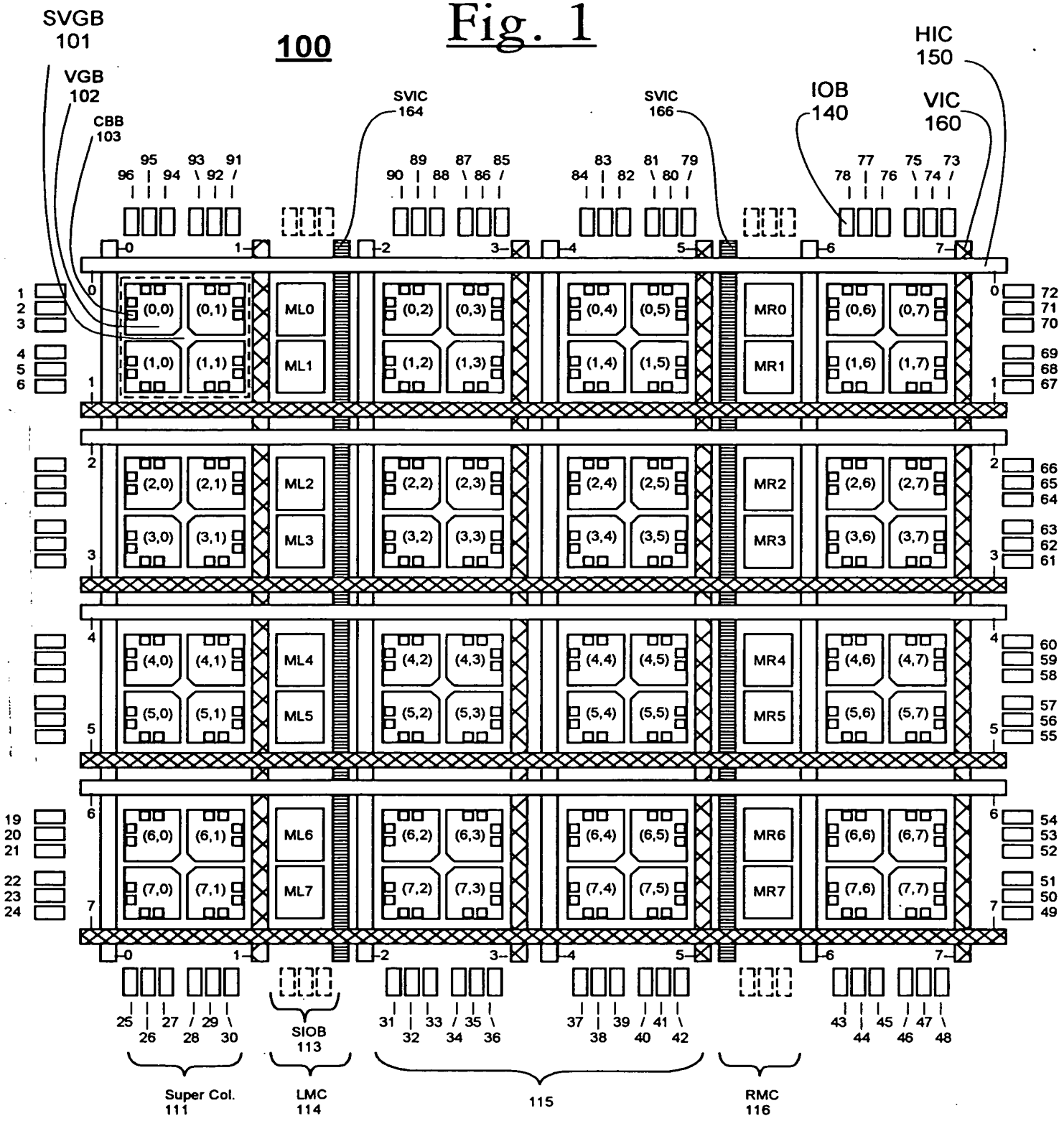
Fig. 1



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15 F19

200

Fig. 2

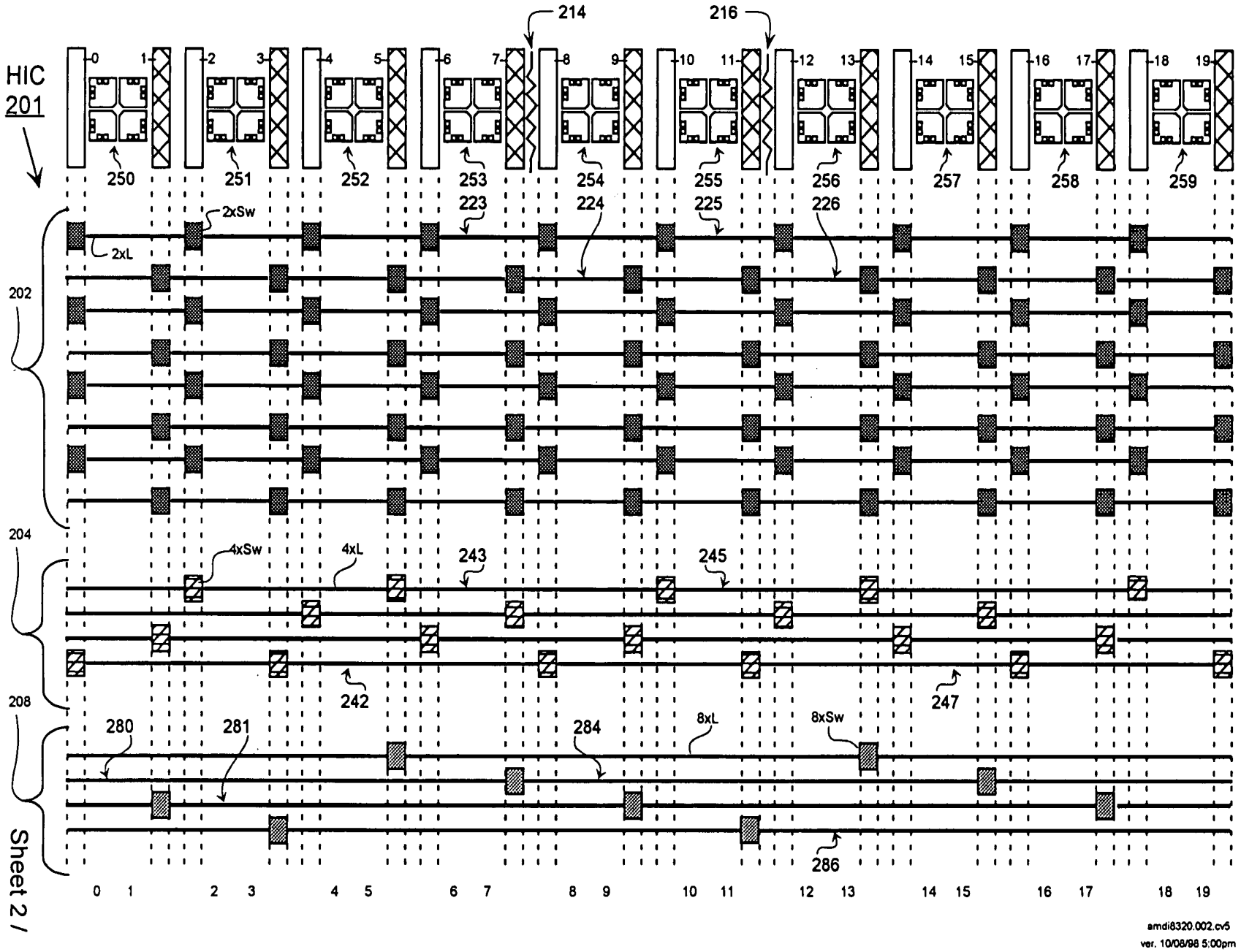

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Fig. 3

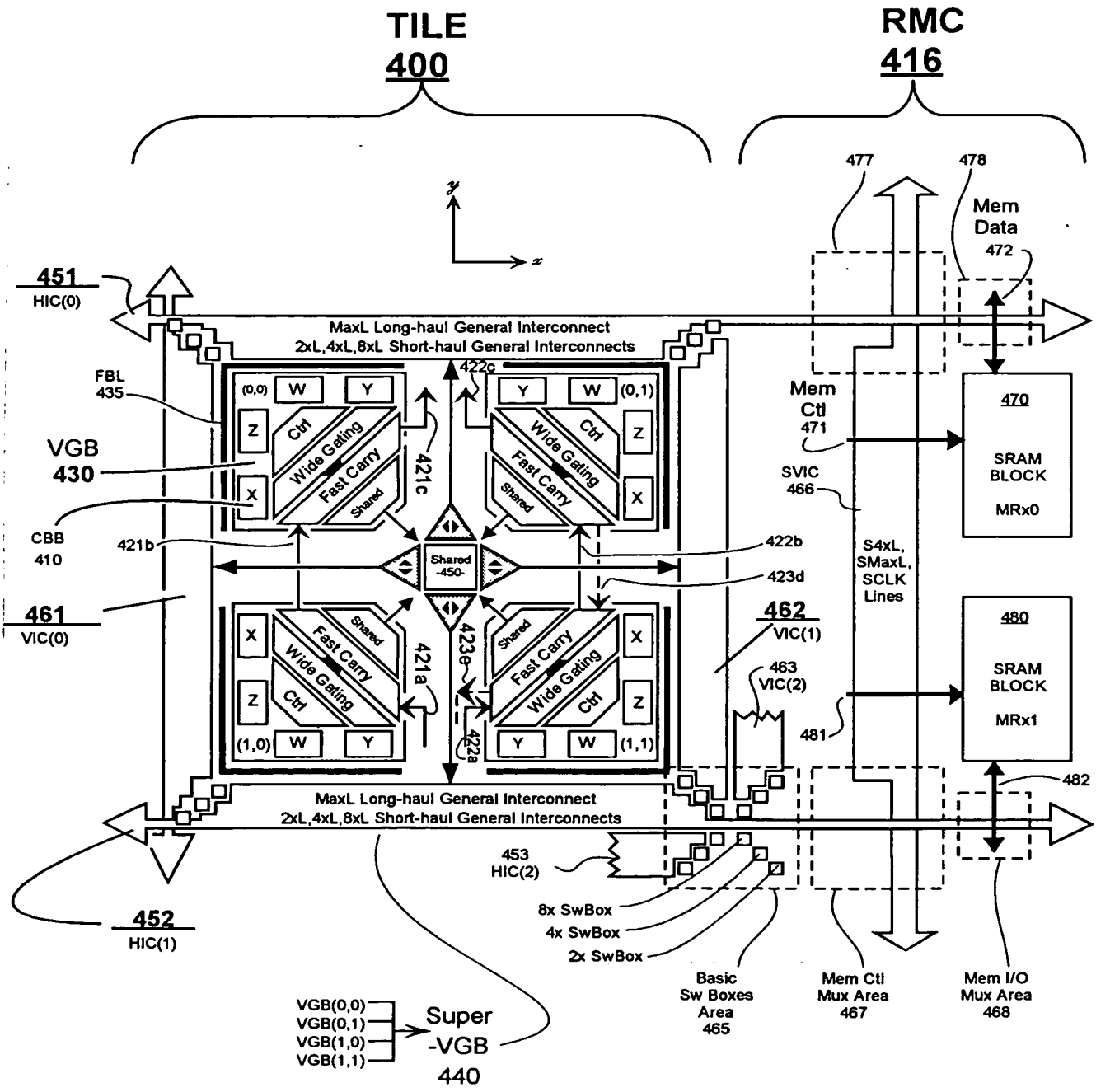
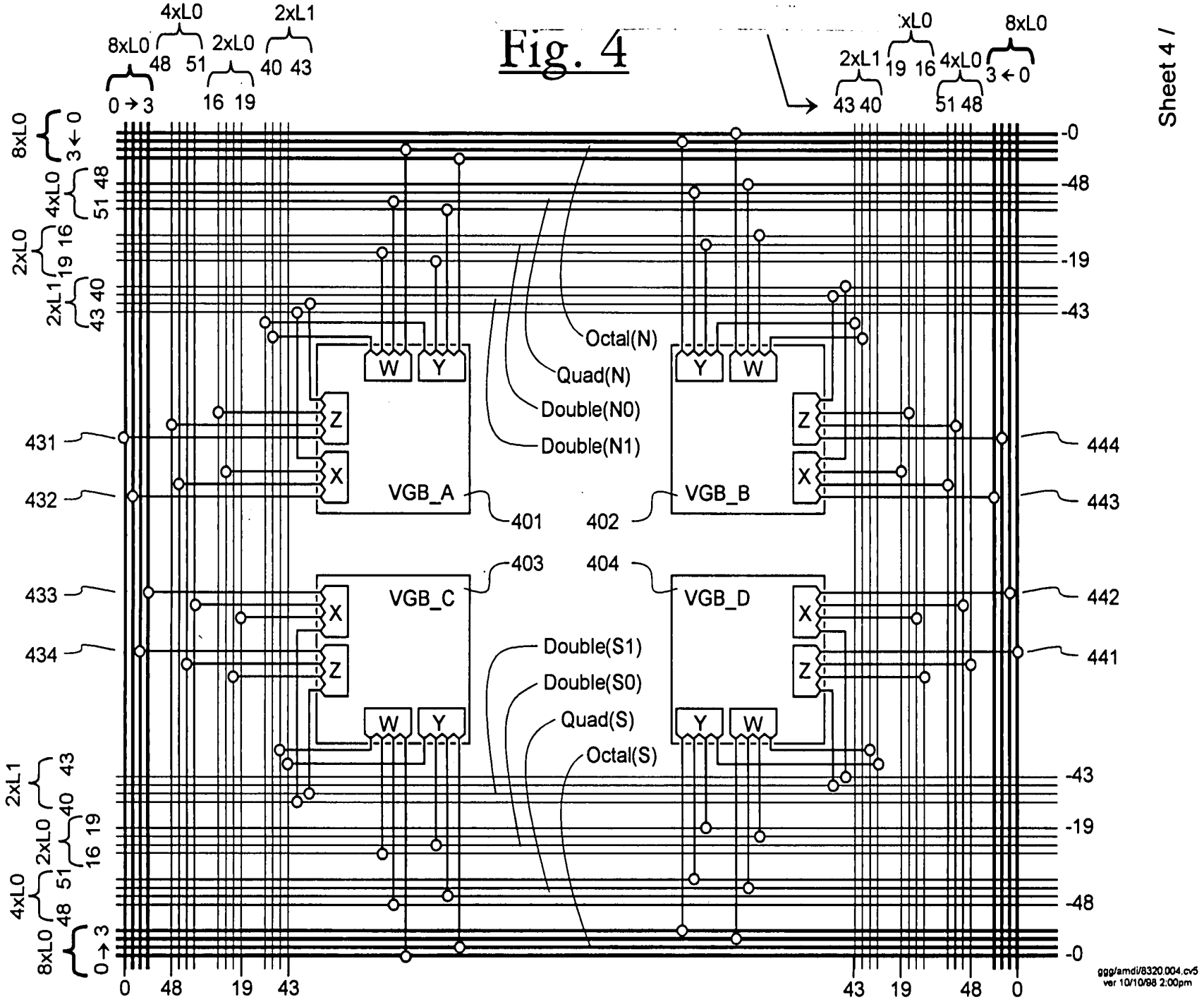

TILE
400
RMC
416
451
HIC(0)
MaxL Long-haul General Interconnect
2xL,4xL,8xL Short-haul General Interconnects
FBL
435
VGB
430
CBB
410
461
VIC(0)
421b
422c
421c
422b
423d
Shared
-450-
421a
423c
422a
462
VIC(1)
463
VIC(2)
481
482
453
HIC(2)
452
HIC(1)
8x SwBox
4x SwBox
2x SwBox
Basic
Sw Boxes
Area
465
Mem Ctl
Mux Area
467
Mem I/O
Mux Area
468
VGB(0,0)
VGB(0,1)
VGB(1,0)
VGB(1,1)
Super
-VGB
440
477
478
Mem
Data
472
Mem
Ctl
471
SVIC
466
470
SRAM
BLOCK
MRx0
480
SRAM
BLOCK
MRx1
S4xL,
SMaxL,
SCLK
Lines
(0,0)
(0,1)
(1,0)
(1,1)
W
Y
Z
X
Ctrl
Wide Gating
Fast Carry
Shared

Fig. 4


4xL0
2xL1
8xL0
48 51
2xL0
40 43
0 → 3
16 19
xL0
8xL0
2xL1
19 16
4xL0
3 ← 0
43 40
51 48
8xL0
3 ← 0
4xL0
48 51
2xL0
16 19
2xL1
40 43
-0
-48
-19
-43
W
Y
Z
X
Octal(N)
Quad(N)
Double(N0)
Double(N1)
431
432
VGB_A
401
402
VGB_B
444
443
403
404
433
434
VGB_C
VGB_D
442
441
Double(S1)
Double(S0)
Quad(S)
Octal(S)
2xL1
43 40
2xL0
16 19
4xL0
51 48
8xL0
0 → 3
0 48 19 43
43 19 48 0
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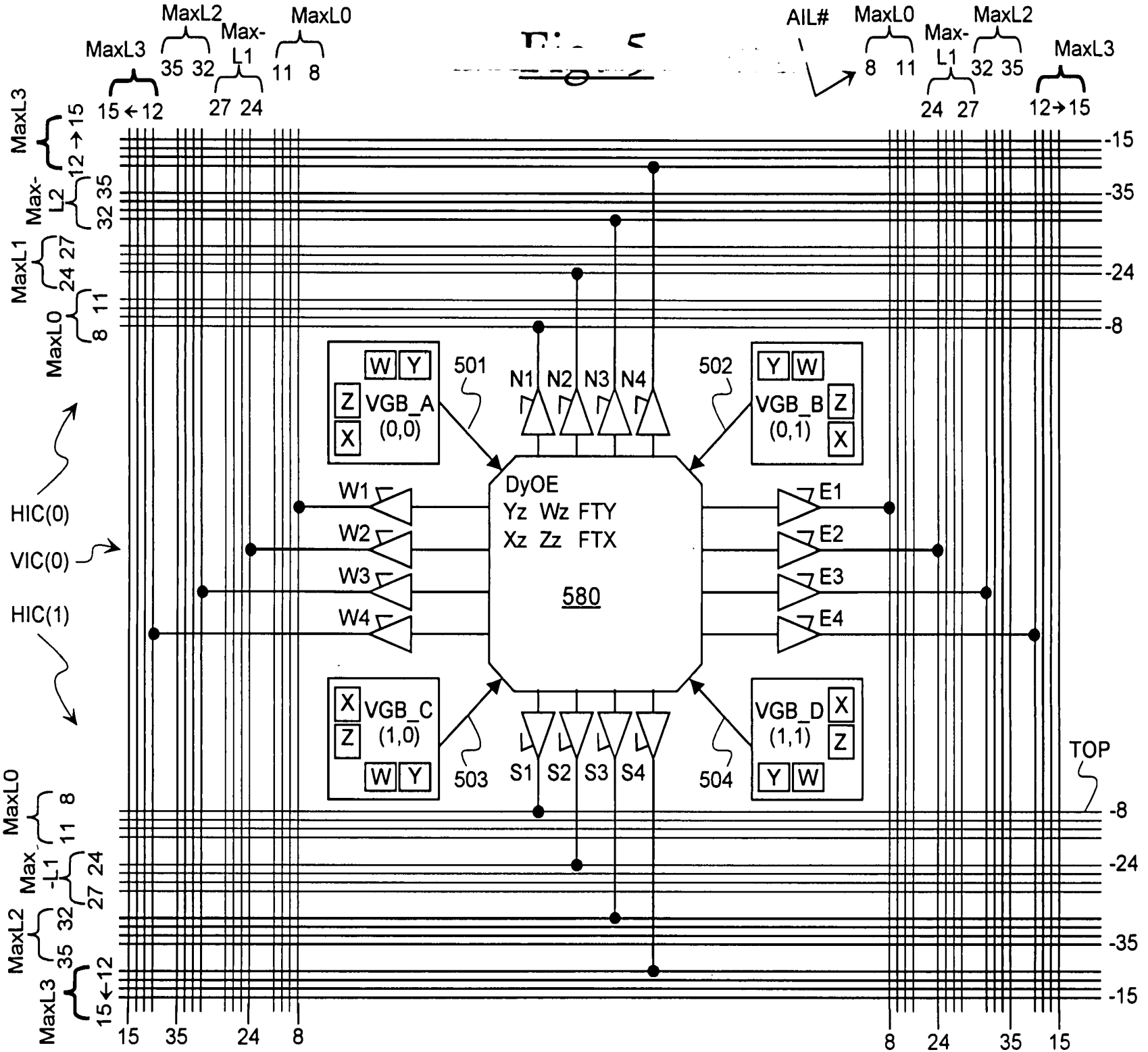
ggg/amd/8320.05.cv5
Tile 1
ver 10/08/98 5:15pm



Sheet 5

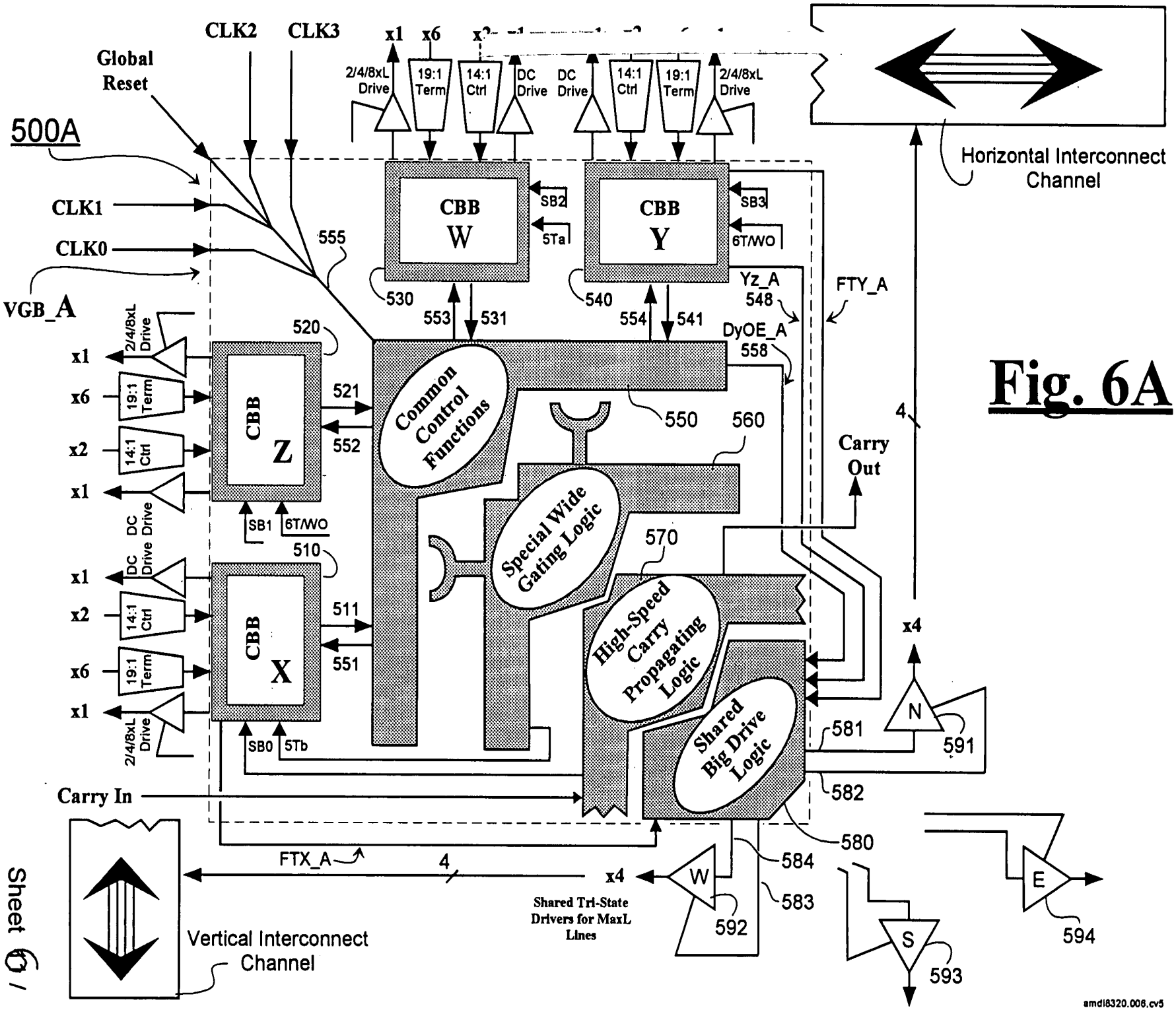

500A
Global Reset
CLK1
CLK0
VGB_A
CLK2
CLK3
x1
x6
x2
x1
2/4/8xL Drive
19:1 Term
14:1 Ctrl
DC Drive
DC Drive
14:1 Ctrl
19:1 Term
2/4/8xL Drive
Horizontal Interconnect Channel
CBB W
CBB Y
CBB Z
CBB X
SB2
5Ta
SB3
6T/WO
SB1
6T/WO
SB0
5Tb
555
520
510
530
540
553
531
554
541
521
552
511
551
Yz_A
548
DyOE_A
558
FTY_A
Common Control Functions
550
560
Special Wide Gating Logic
570
High-Speed Carry Propagating Logic
Shared Big Drive Logic
Carry Out
4
x4
N
581
591
582
580
584
583
Carry In
FTX_A
4
x4
Shared Tri-State Drivers for MaxL Lines
W
592
S
593
E
594
Vertical Interconnect Channel
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Fig. 6A

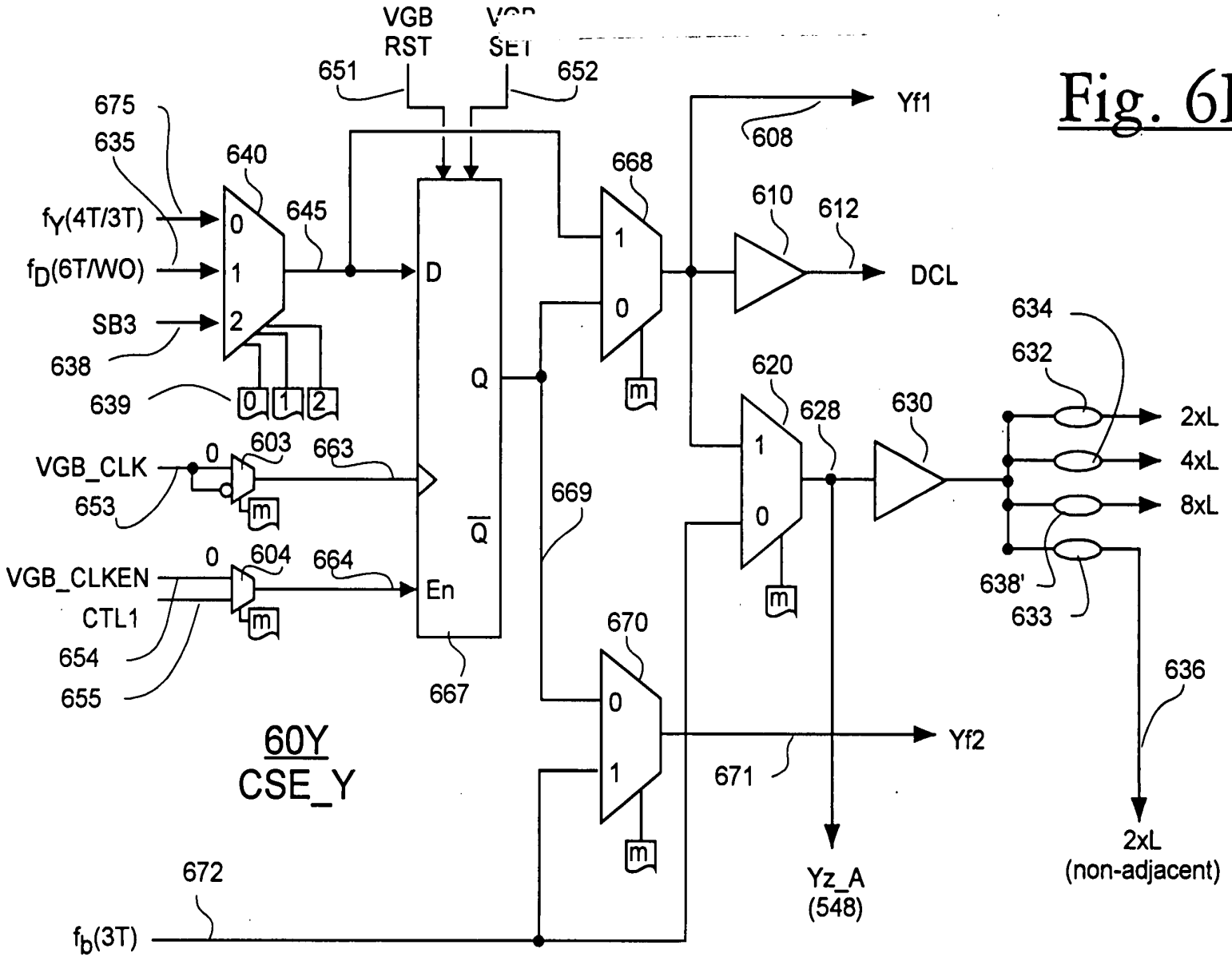

Fig. 6B

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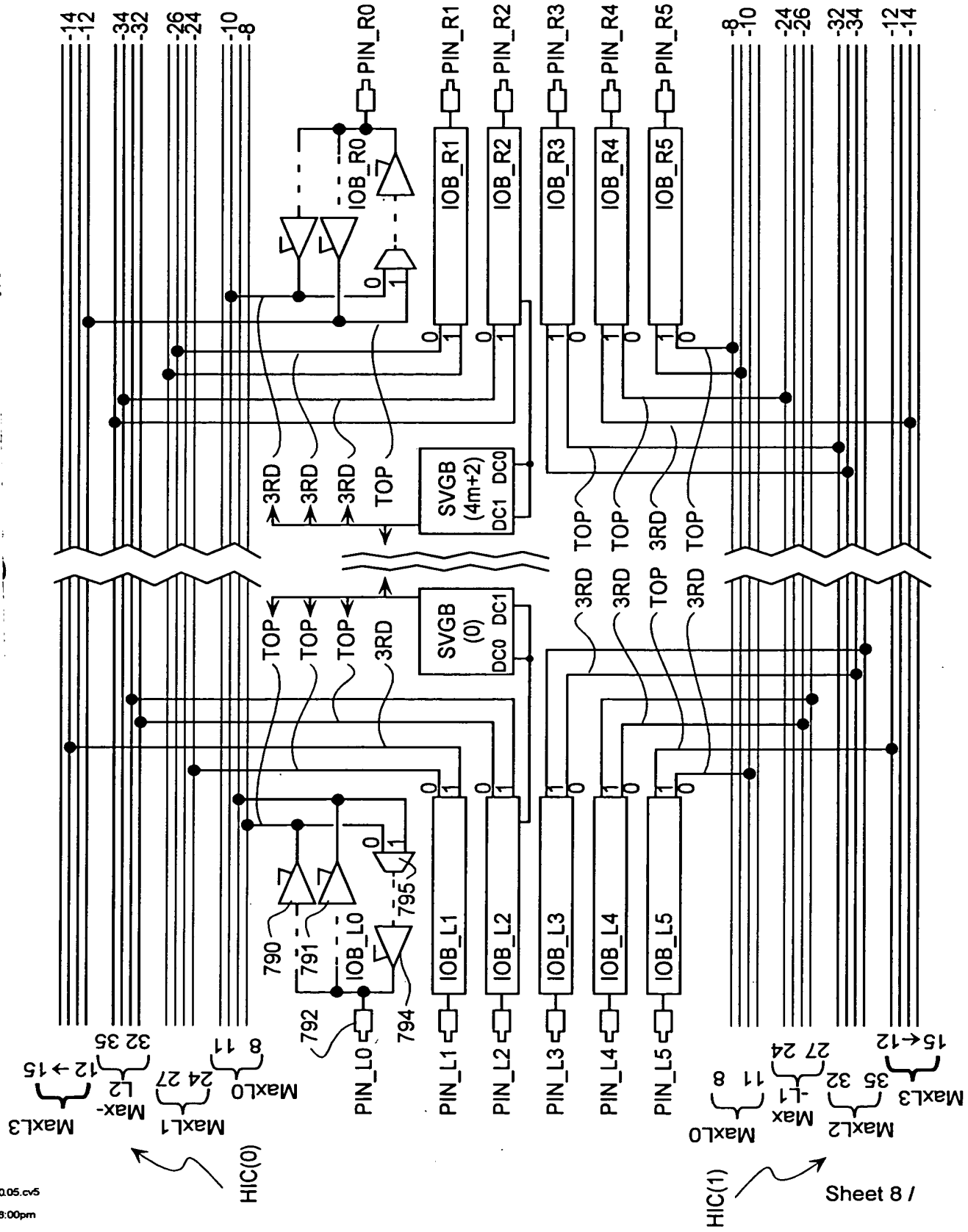
Fig 7A



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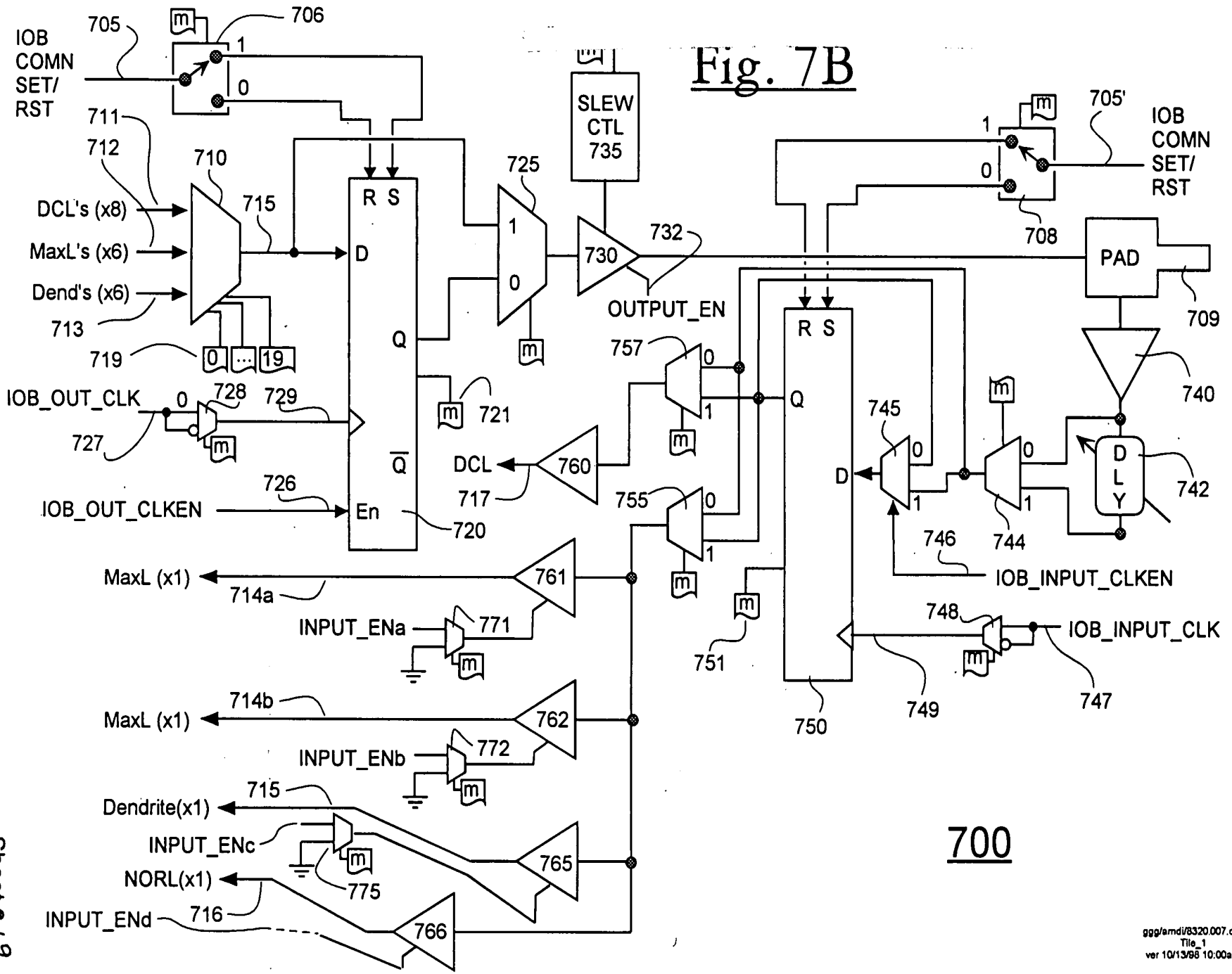

Fig. 7B

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ver 10/13/98 10:00am

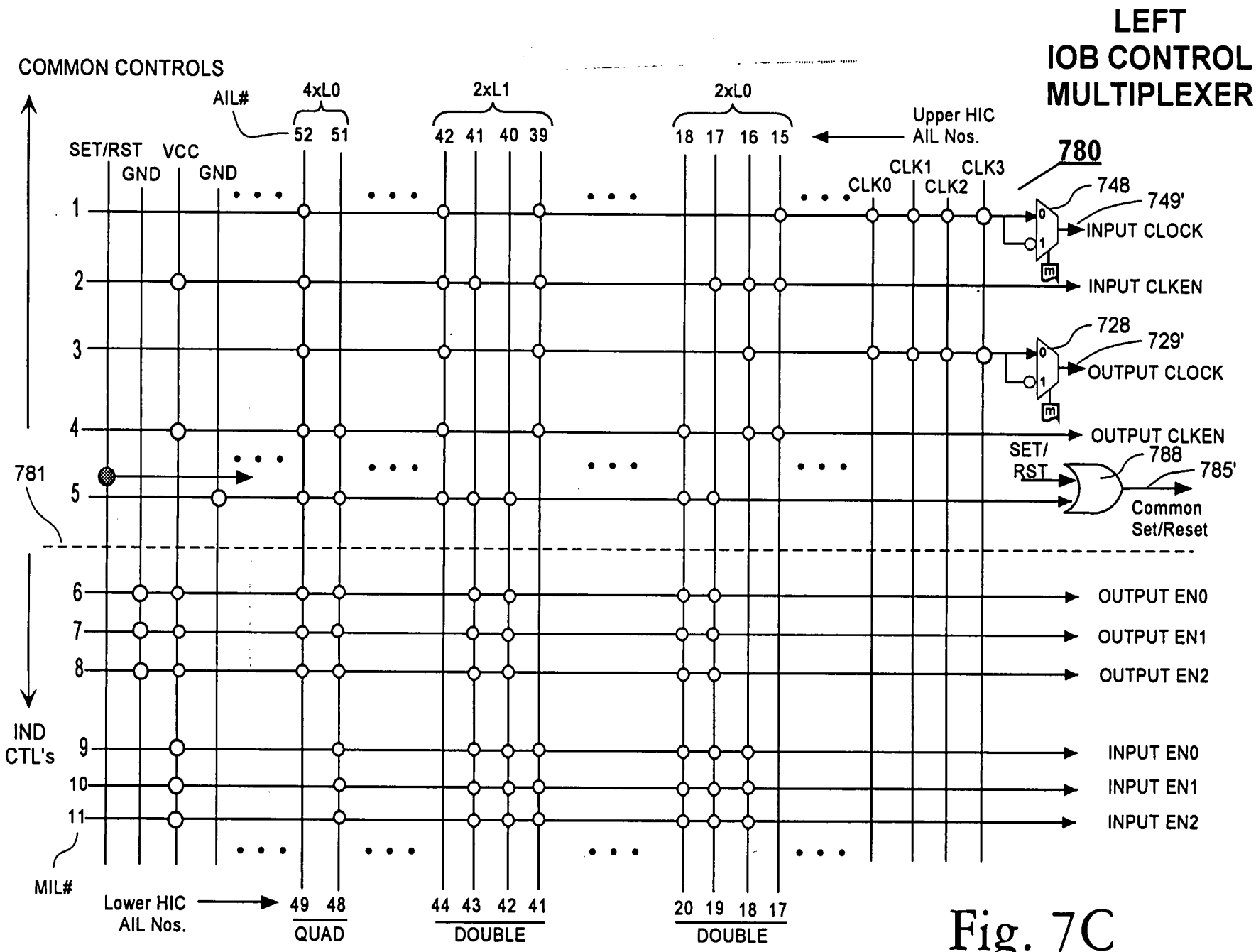

Fig. 7C

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Fig. 8

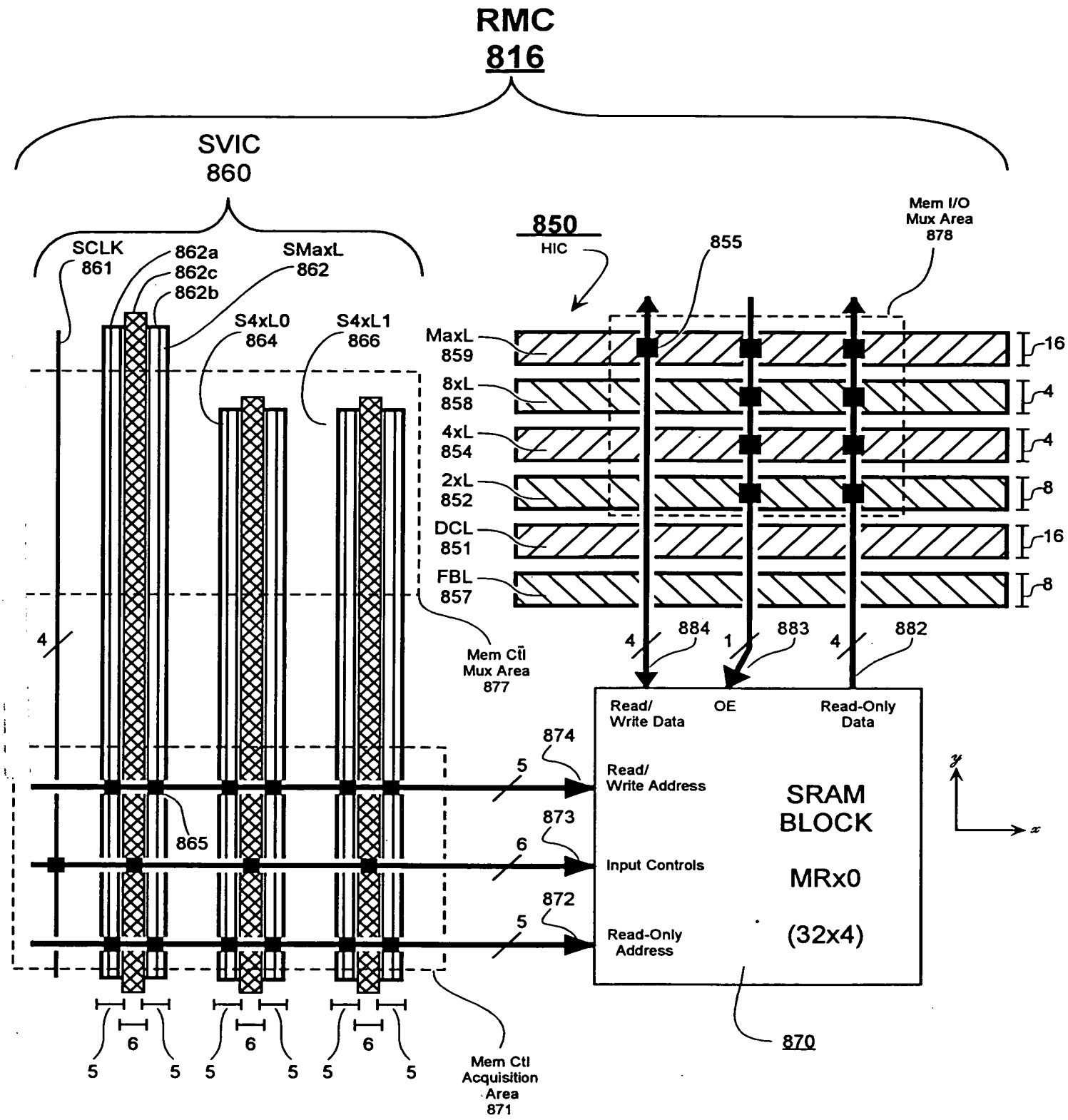

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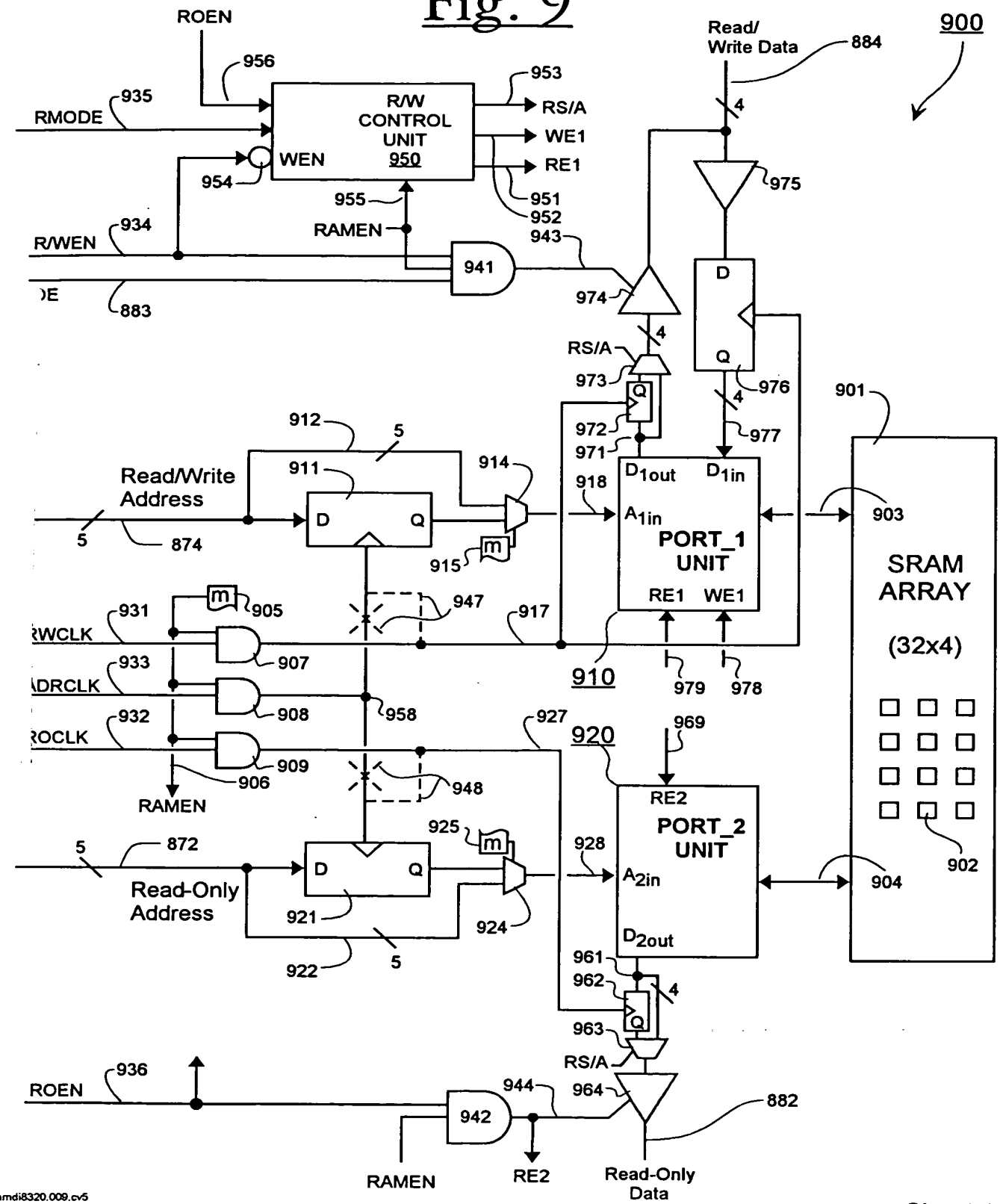
Fig. 9



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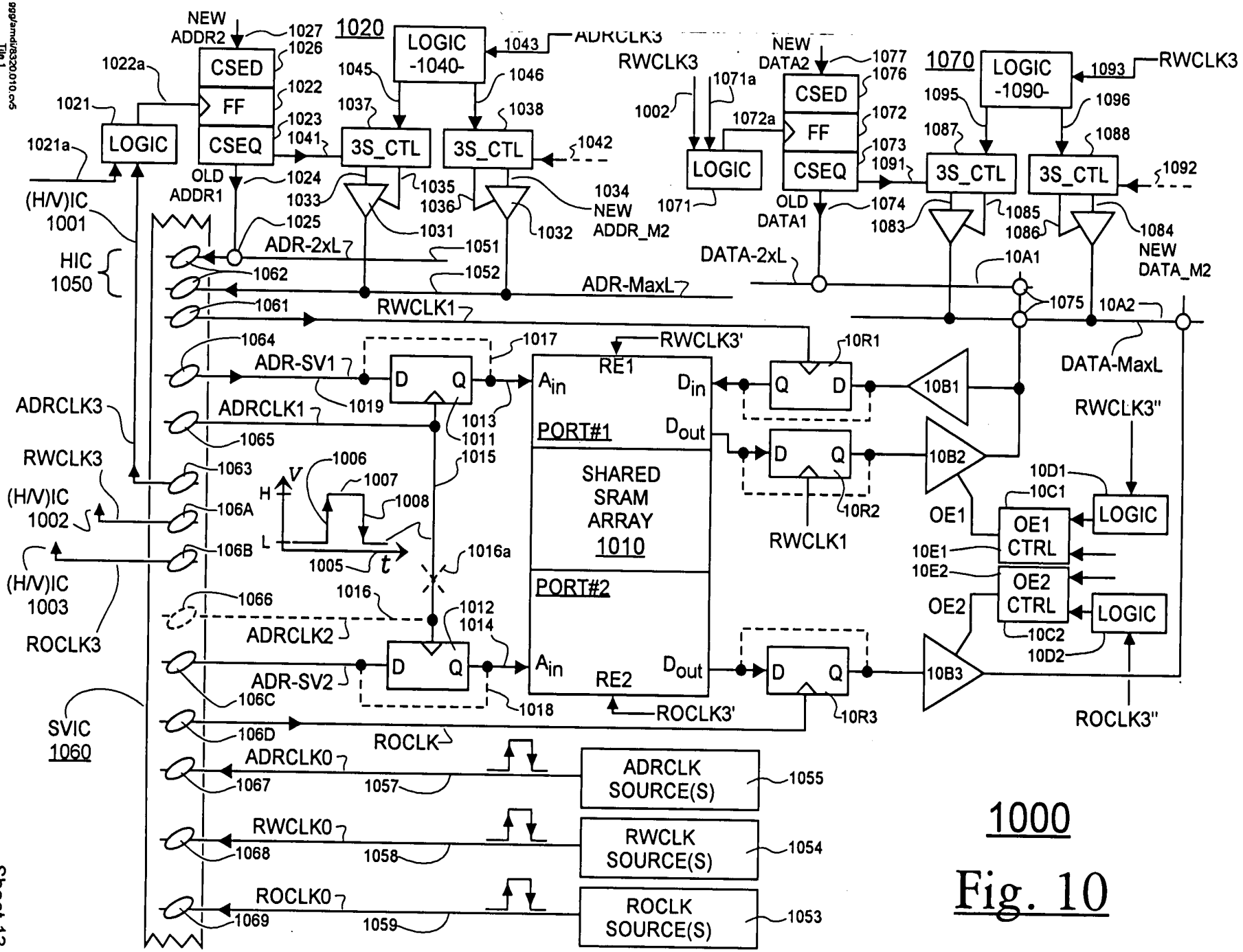


Fig. 10

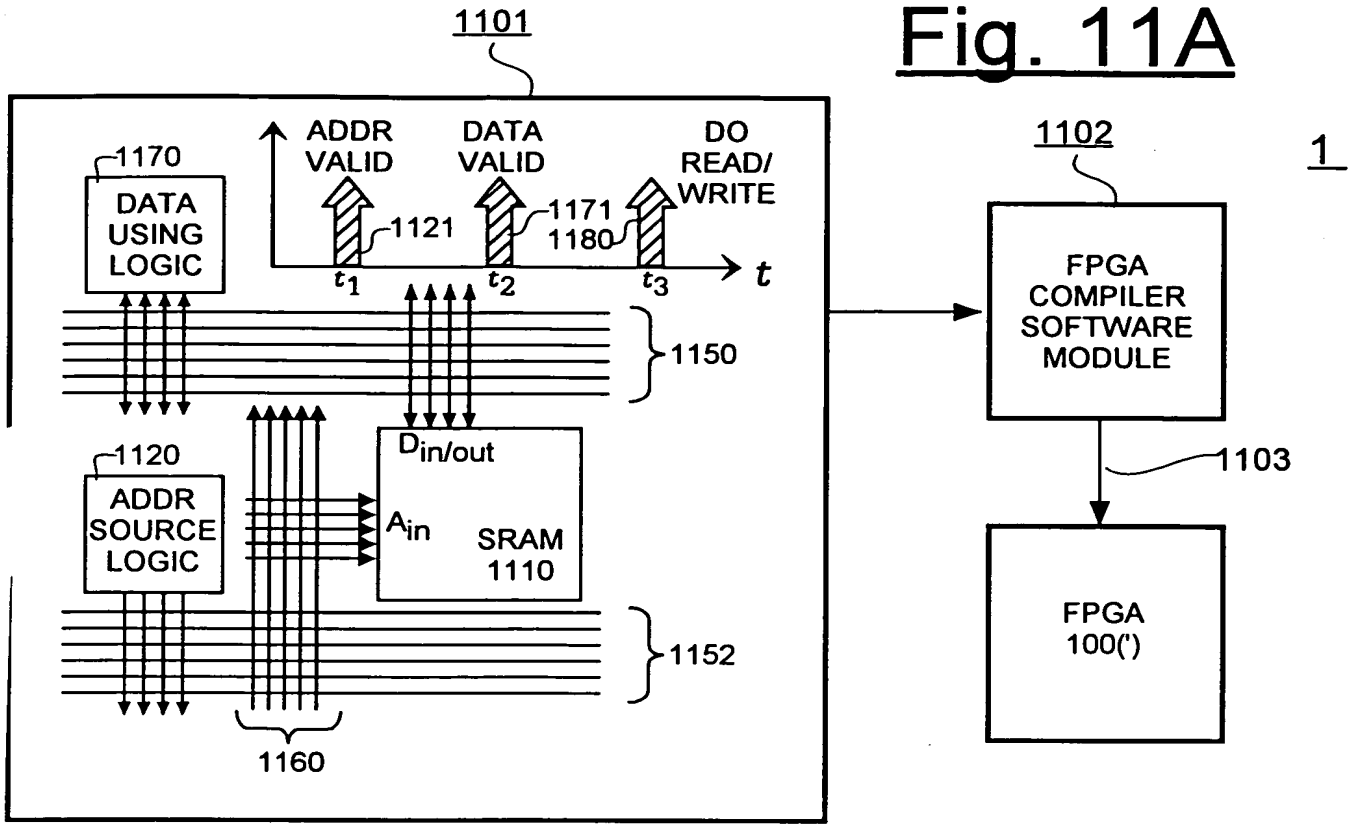
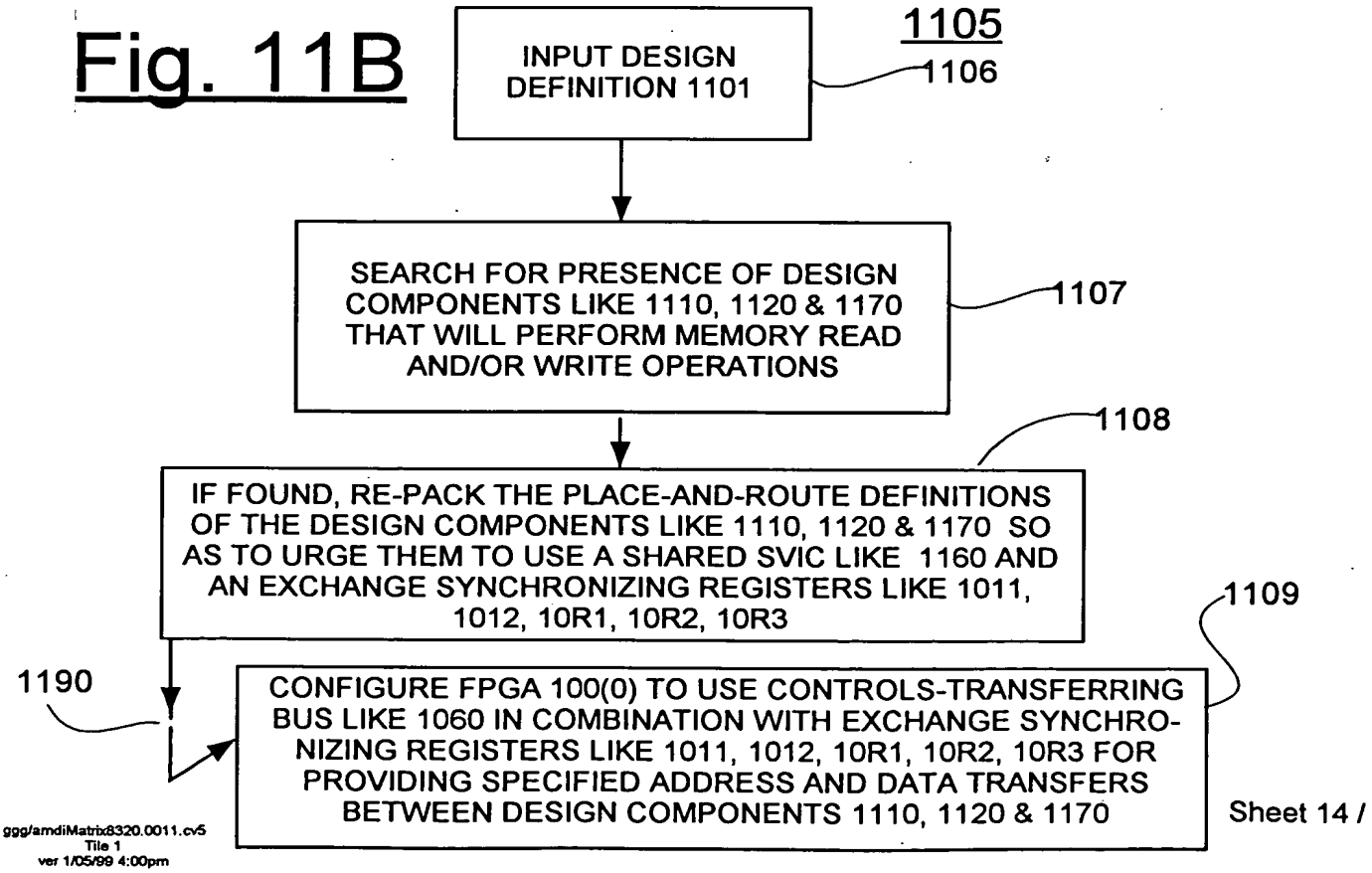


Fig. 11A

Fig. 11B



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ver 1/05/99 4:00pm